Course Code: 20EC0412 **R20**

SIDDHARTH GROUP OF INSTITUTIONS: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583
QUESTION BANK (DESCRIPTIVE)

Subject with Code: AVLSI (20EC4212) **Course & Branch**: M.Tech –VLSI
Regulation: R20 **Year & Sem:** I-M.Tech & II-Sem

UNIT –I

PRELIMINARIES

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

1. (a)What are the most important entities in VLSI design and explain in detail? [L2][CO1][5M]
   (b)Draw the decomposition tree and explain. [L3][CO1][7M]

2. (a)How combinational optimization is achieved using Local and Tabu search? [L3][CO1][6M]
   (b)Explain the following: (i) Backtracking. (ii) Branch and bound programming [L1][CO1][6M]

3. (a) Explain the different design automation tools for VLSI design [L1][CO1][6M]
   (b)Explain algorithms for constrained graph compaction [L1][CO3][6M]

4. Explain about the design methodology based on top-down structural decomposition and bottom up Layout reconstruction using Gajski's y-chart. [L2][CO1][12M]

5. What are the several purpose methods for combinational optimization?
   Explain briefly. [L1][CO1][12M]

6. (a)What is the importance of design automation tools. [L2][CO3][3M]
   (b) Describe any three design automation tools [L3][CO2][9M]

7. (a)Analyze what is the need of genetic algorithm. [L4][CO3][6M]
   (b)Explain about Genetic Algorithms. [L1][CO1][6M]

8. Write about the combinatorial optimization problems and decision problems. [L1][CO1][12M]

9. Design dynamic programming approach for travelling salesman problem [L3][CO3][12M]

10. With example explain briefly tractable and intractable problems related to VLSI design automation [L1][CO3][12M]

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UNIT-II

LAYOUT COMPACTION

MODELLING AND SIMULATION

1. Explain briefly the following:
   (a)The concept of placement in VLSI design. [L1][CO2][6M]
   (b)The routing problems and routing techniques in VLSI design. [L1][CO2][6M]

2. (a)With an example, explain the difference between modeling and simulation. [L1][CO3][6M]
   (b) Explain Gate level and switch level modeling. [L2][CO3][6M]

3. (a)What is floor planning? [L2][CO2][6M]
   (b) Compare the compiler driven simulation and event driven simulation [L2][CO3][6M]

4. (a)What is layout compaction? Explain algorithms for constrained graph compaction [L2][CO2][6M]
   (b) Explain about the important abstraction levels that are necessary for a specific simulation tool. [L2][CO2][6M]

5. (a) What is the placement? What is the requirement of placement? [L2][CO2][5M]
   (b) Explain the concept of placement with respect to layout synthesis. [L2][CO2][7M]

6. What is meant by modeling and simulation? Differentiate gate level and switch level modeling and simulation procedures with suitable example [L2][CO2][12M]

7. (a)What is the concept of layout compaction and clearly explain how compaction is useful for VLSI design? [L2][CO2][6M]
   (b)Explain with an algorithm how routing problems can be overcome? [L2][CO2][6M]

8. (a)Summarize the important abstraction levels that are necessary for a specific simulation tool [L3][CO3][6M]
   (b)Discuss about the compiler driven simulation and event driven simulation. [L3][CO3][6M]

9. With suitable examples explain the switch level modeling and simulation [L3][CO3][12M]

10. Explain the routing problems in floor planning methods of VLSI design. [L1][CO2][12M]

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UNIT III

LOGIC SYNTHESIS AND VERIFICATION

1. (a) Draw Binary-Decision diagrams for an Inverter [L3][CO3] [6M]
   (b) Write short notes of logic synthesis [L2][CO3] [6M]

2. (a)What are the principles of reduced ordered binary decision diagram? [L2][CO3] [6M]
   (b)What are the issues and terminology involved in the combinational logic synthesis [L2][CO3] [6M]

3. (a)Explain ROBDD implementation and construction [L1][CO3] [6M]
   (b)With example explain the ROBDD manipulation? [L3][CO3] [6M]

4. Explain Heuristic based on ROBDD? [L2][CO3] [12M]

5. (a) What is the principle of ROBDD? [L2][CO3] [4M]
   (b) Explain how OBDD size is reduced to obtain ROBDD? [L1][CO3] [4M]
   (c) Explain how ROBDDS can be used for logic verifications? [L1][CO3] [4M]

6. (a) What is a combinational logic synthesis? [L2][CO3] [6M]
   (b) With practical example explain the combinational logic synthesis? [L3][CO4] [6M]

7. Explain the following
   (a)ROBDD principles [L1][CO4] [6M]
   (b)ROBDD implementation and construction [L1][CO4] [6M]

8. Explain the following related to ROBDD
   (a) Variable ordering [L2][CO3] [6M]
   (b) Applications to verification [L2][CO3] [6M]

9. Explain how ROBDD can be used for combitorial optimization [L1][CO3] [12M]

10. (a) What is two level logic synthesis [L2][CO3] [4M]
    (b)Explain problem definition and analysis in two level logic synthesis [L1][CO3] [8M]

UNIT –IV

HIGH-LEVEL SYNTHESIS

1. (a) List & explain any two scheduling algorithms. [L3][CO4] [6M]
   (b) Describe High-level Transformation [L1][CO4] [6M]

2. (a) Explain the Force-directed scheduling in detail. [L1][CO4] [6M]
   (b) Write about the Hardware models for High-level synthesis. [L2][CO4] [6M]

3. (a) What is the internal representation of the input algorithm? [L2][CO4] [4M]
   (b)Explain any three methods [L1][CO4] [8M]

4. Explain the following algorithms
   (a) ASAP algorithm. [L1]CO4][6M]
   (b) Mobility based scheduling. [L1][CO4][6M]

5. (a) What type of Hardware components can be used by a high- level synthesis system? [L2][CO4][6M]
   (b) Explain how the ASAP scheduling algorithm is used to find the longest path?[L1][CO4][6M]

6. With detailed example explain the allocation, assignment and scheduling [L3][CO5][12M]

7. Explain the following algorithms
   (a) Force directed scheduling [L1][CO5][6M]
   (b) List scheduling [L1][CO5][6M]

8. What are the aspects of assignment problem? Explain. [L2][CO4][12M]

9. (a) Explain the high-level transformations. [L1][CO4][6M]
   (b)Explain dataflow graph representation. [L1][CO4][6M]

10. Explain the following algorithms
    (a) Simple dataflow [L1][CO4][4M]
    (b) Conditional dataflow [L1][CO4][4M]
    (c) Iterative dataflow [L1][CO4][4M]

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UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S

PHYSICAL DESIGN AUTOMATION OF MCM'S

1. (a)Explain the physical design cycle of FPGA [L1][CO5][6M]
   (b) How partitioning is performed for staggered model [L3][CO5][6M]

2. Write short notes on the following:
   (a)Maze routing [L3][CO6][6M]
   (b)Programmable MCM's [L3][CO6][6M]

3. (a) Explain the types of logic blocks for FPGA with neat sketches [L1][CO5][6M]
   (b)Develop a routing algorithm for the non-segmented model. [L6][CO5][6M]

4. (a) With neat sketch explain about the physical design cycle of MCM. [L3][CO5][6M]
   (b)Briefly explain about the different approaches to be followed for General MCM routing problems. [L1][CO6][6M]

5. (a) Explain the FPGA technologies. [L2][CO5][6M]
   (b) How partitioning is performed for segmented model [L3][CO5][6M]

6. (a)Briefly explain MCM technologies. [L2][CO6][6M]
   (b) What are the different methods of MCM routing? Explain. [L2][CO6][6M]

7. Explain the types of logic blocks and routing models for FPGA with neat sketches [L1][CO5][12M]

8. Explain the following routing algorithms
   (a)Topological routing [L1][CO5][6M]
   (b)Integrated pin distribution and routing [L1][CO5][6M]

9. (a)How the routing network is modeled in FPGA? [L3][CO5][6M]
   (b) Discuss the routing Algorithm for staggered model and compare it with segmentation model. [L3][CO5][6M]

10. (a) What are the various steps in MCM physical design cycle? Explain them briefly. [L2][CO5][6M]
    (b) Explain the method of topological routing for general MCM. [L1][CO5][6M]

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